4,194,304 WORD X 4 BIT DYNAMIC RAM

DESCRIPTION

The TC5116400J/FT is the new generation dynamic RAM organized 4,194,304 word by 4 bit. The TC5116400J/FT utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC5116400J/FT to be packaged in a 28/24 pin plastic SOJ, and 28/24 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 4,194,304 word by 4 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in V_{BB} generator
- Low Power
  495mW MAX .Operating
  (TC5116400J/FT-60)
  440mW MAX. Operating
  (TC5116400J/FT-70)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 4096 refresh cycles/64ms
- Package TC5116400J : SOJ28-P-400A
  TC5116400FT : TSOP28-P-400B

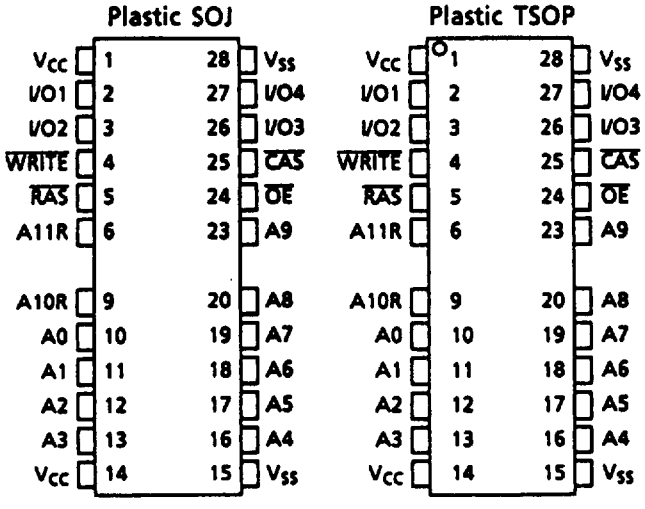
KEY PARAMETERS

ITEM		TC5116400J/FT	
		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{AA}	Column Address Access Time	30ns	35ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

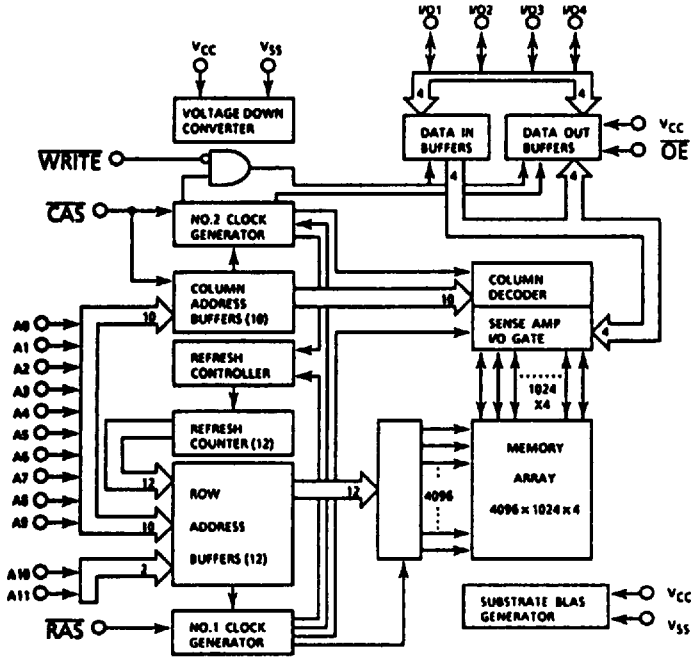
PIN NAME

A0~A11	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	V_{CC}+0.5	V	2
V_{IL}	Input Low Voltage	-0.5*	-	0.8	V	2

*-2.0V at pulse width ≤ 20ns

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC511640J/FT-60	-	90	mA	3,4 5
		TC511640J/FT-70	-	80		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC511640J/FT-60	-	90	mA	3, 5
		TC511640J/FT-70	-	80		
			-			
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$, Address Cycling:t_{PC}=t_{PC} MIN.)	TC511640J/FT-60	-	70	mA	3,4 5
		TC511640J/FT-70	-	60		
			-			
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	TC511640J/FT-60	-	90	mA	3, 5
		TC511640J/FT-70	-	80		
			-			
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤V_{CC}, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤V_{CC})		-10	10	μA	
V_{OH}	OUTPUT CURRENT Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT CURRENT Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	TC5116400J/FT				UNIT	NOTES
		-60		-70			
		MIN	MAX.	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	ns	
t_{RMW}	Read-Modify-Write Cycle	155	-	180	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	45	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	85	-	95	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	15	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	-	35	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	40	-	50	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	70	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	15	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	-	40	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	30	-	35	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC5116400J/FTL				UNIT	NOTES
		-60		-70			
		MIN	MAX	MIN	MAX		
t_{WCH}	Write CommandHold Time	10	-	15	-	ns	
t_{WP}	Write Command Pulse Width	10	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	10	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	10	-	15	-	ns	12
t_{REF}	Refresh Period	-	64	-	64	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	40	-	45	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	85	-	95	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	55	-	60	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	60	-	65	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	20	-	30	-	ns	
t_{ROH}	RAS Hold Time referenced to OE	10	-	10		ns	
t_{OEA}	OE Access TIme	-	15		20	ns	
t_{OED}	OE to Data Delay	15	-	15	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from OE	0	15	0	15	ns	10
t_{OEH}	OE Command Hold Time	15	-	15	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{WRH}	$\overline{Write}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle	10	-	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	TC5116400J/FTL				UNIT	NOTES
		-60		-70			
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	115	-	135	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	65	-	75	ns	9,14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	25	ns	9,14
t_{AA}	Access Time from Column Address	-	35	-	40	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	75	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	200,000	75	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	-	75	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold	40	-	45	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead	35	-	40	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20		25	ns	
t_{RAL}	$\overline{OE}$ Command Hold Time	30	-	20	-	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A11)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	pF
C_O	Input Capacitance (I/O1~I/O4)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

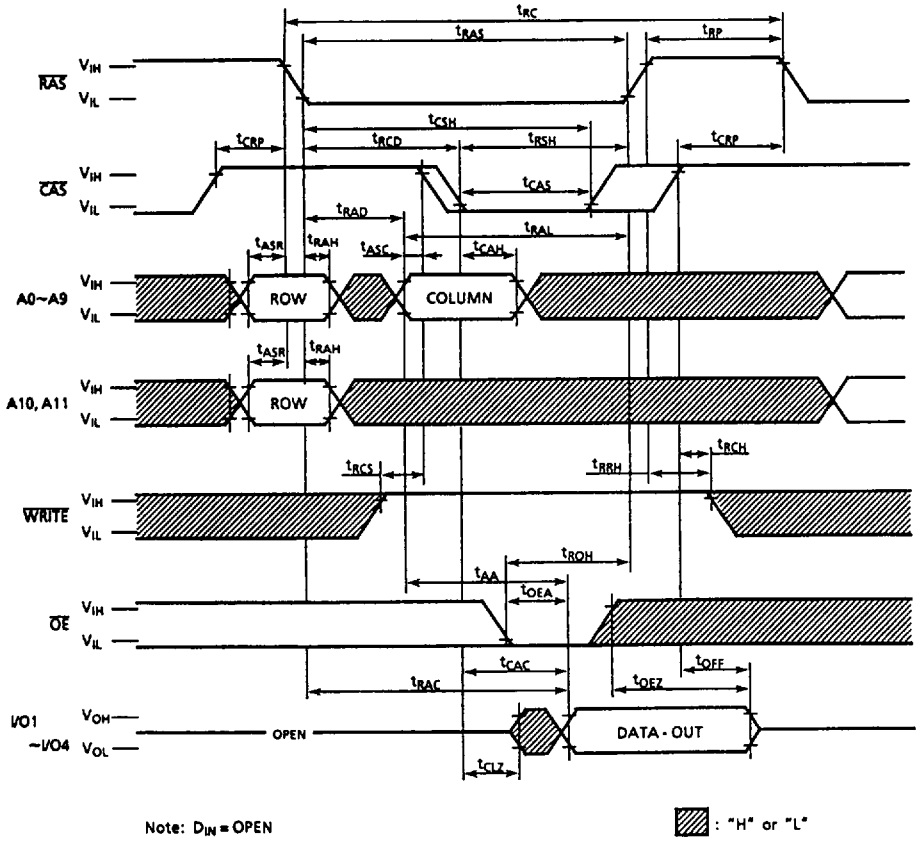
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the date sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} > t_{RWD}$ (min.), $t_{CWD} > t_{CWD}$ (min.), $t_{AWD} > t_{AWD}$ (min.) and $t_{CPWP} > t_{CPWDD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

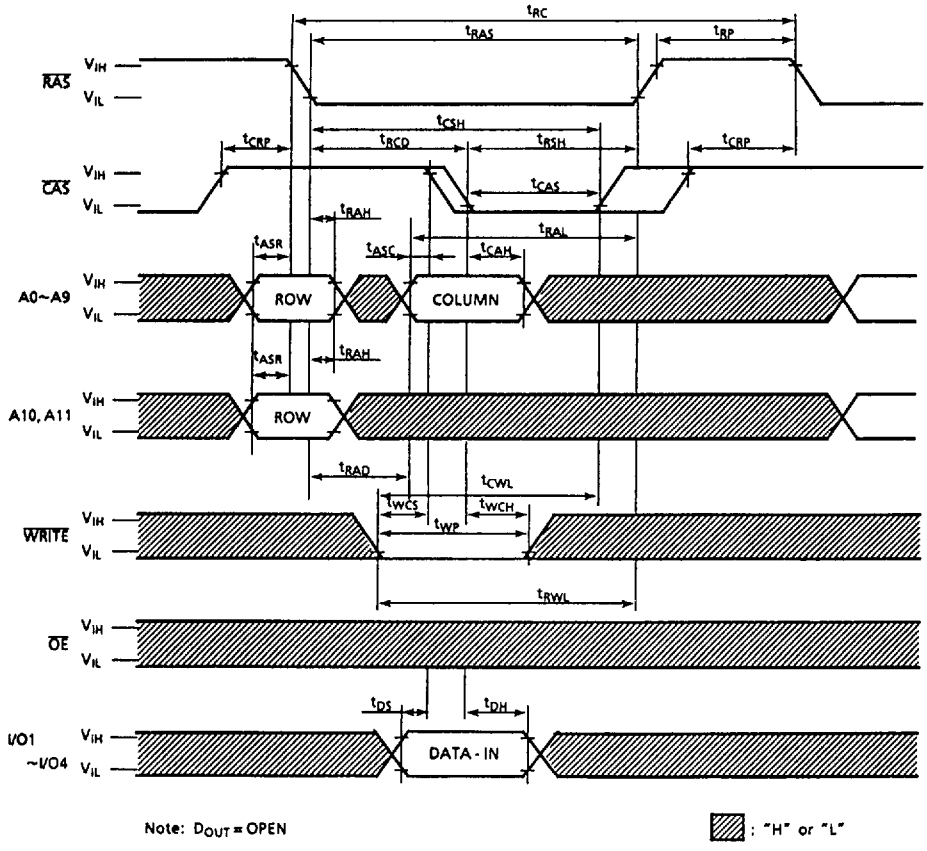
READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

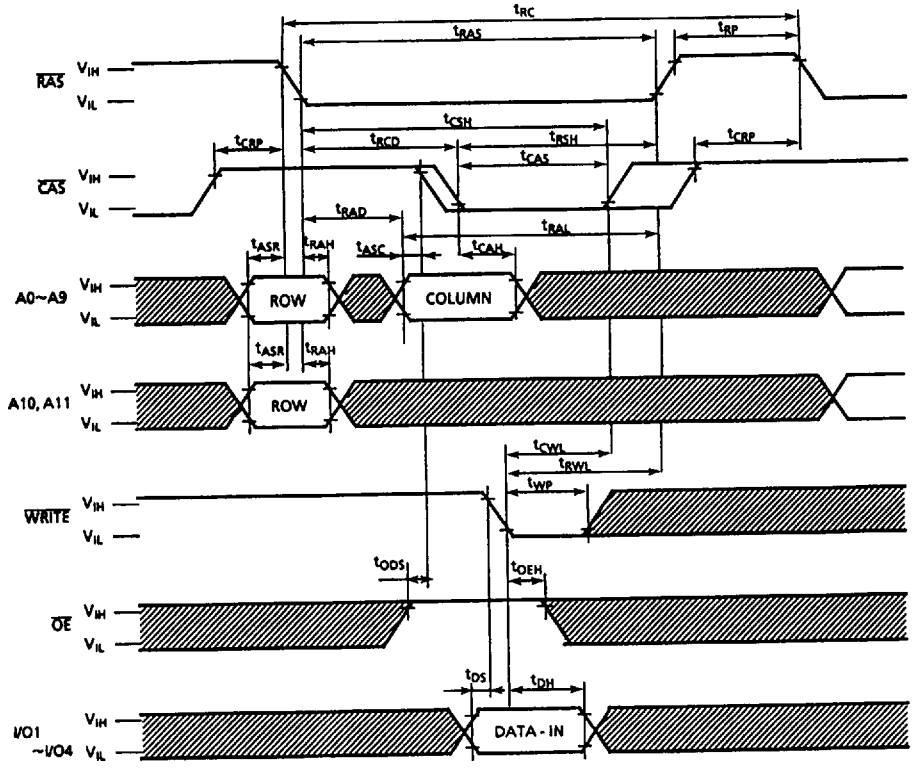
WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

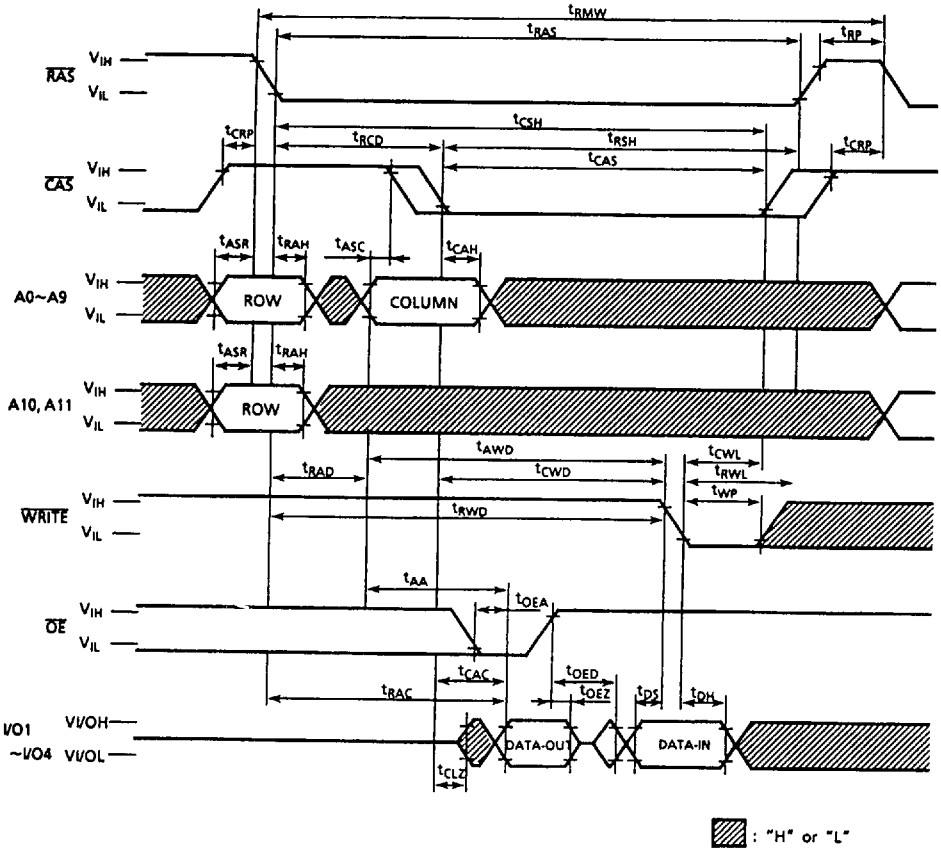
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



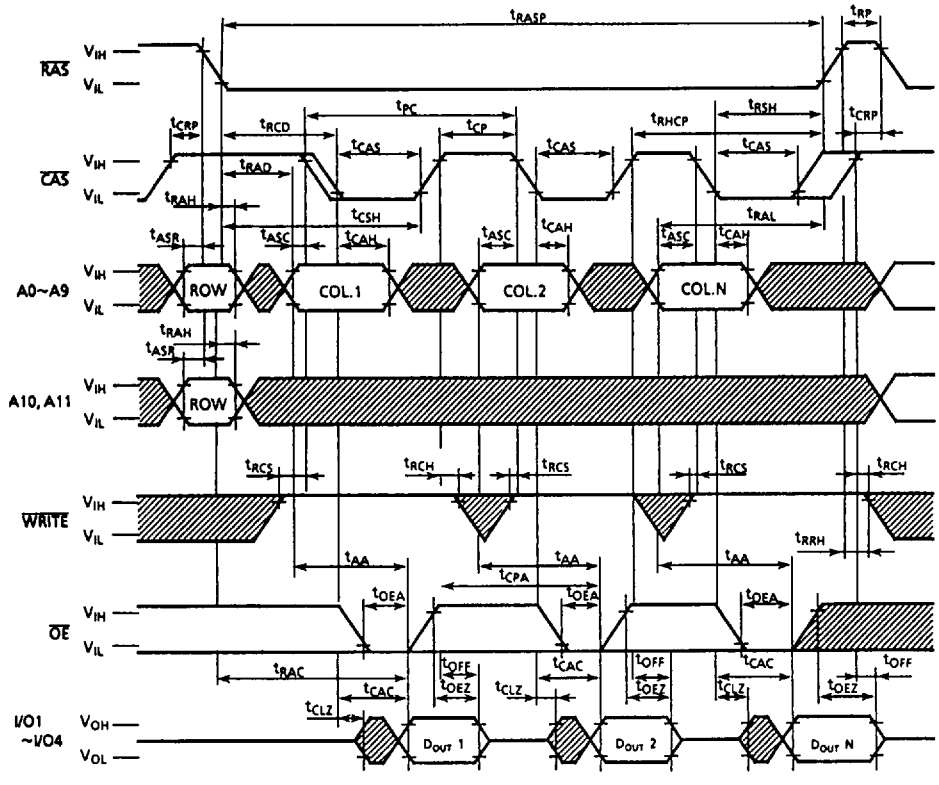
Note: D_{OUT} = OPEN

▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE



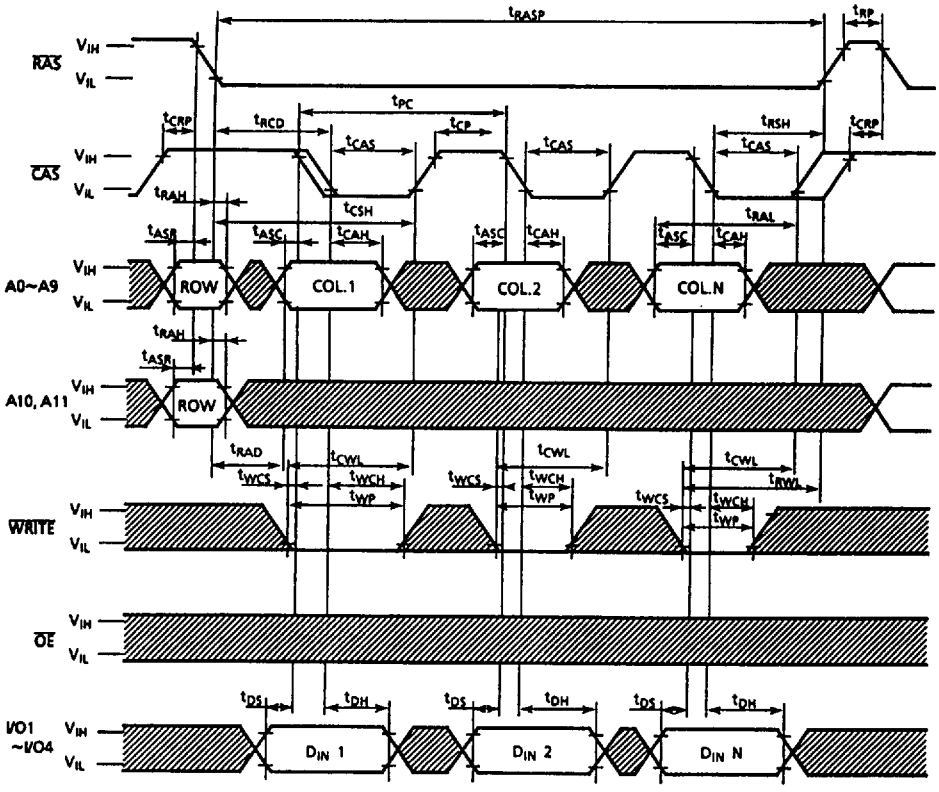
FAST PAGE MODE READ CYCLE



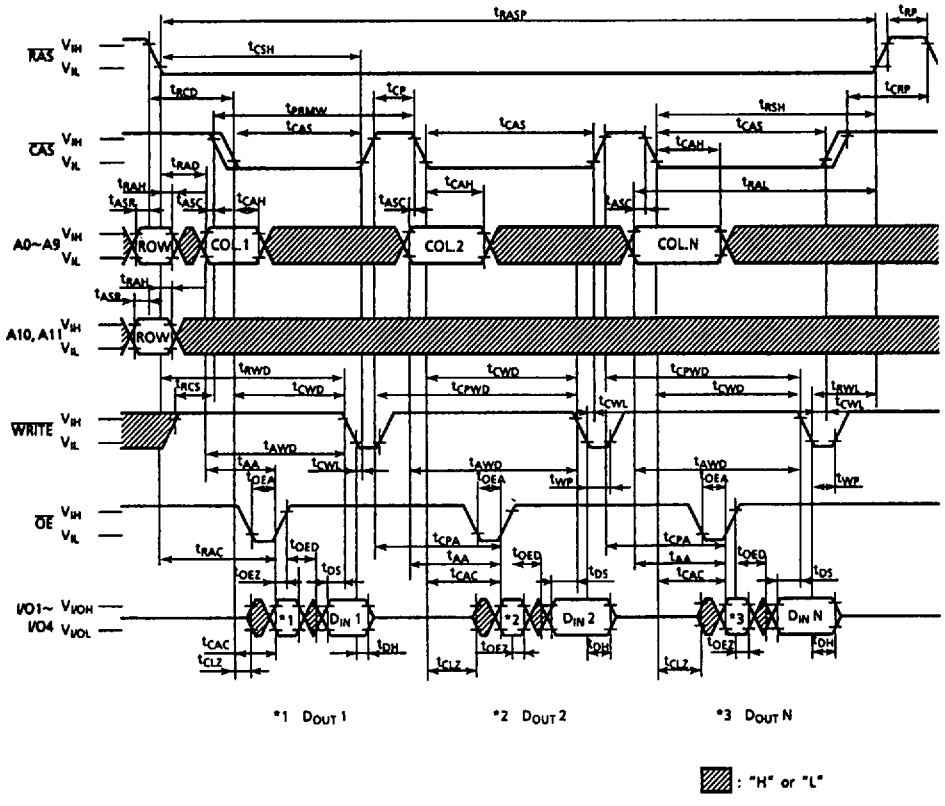
Note: D_{IN} = OPEN

▨ : "H" or "L"

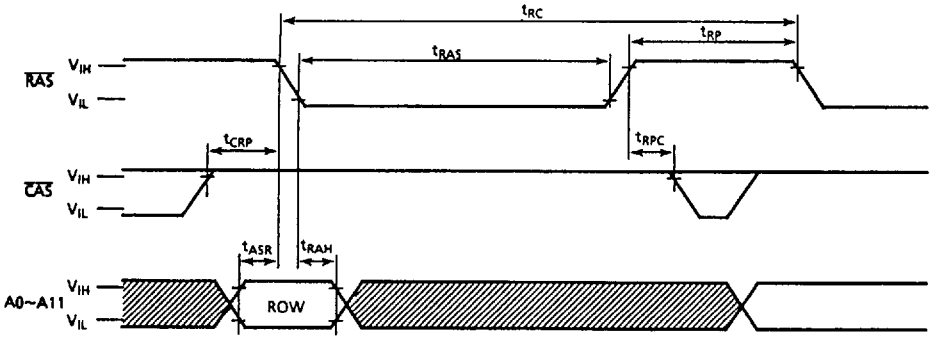
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



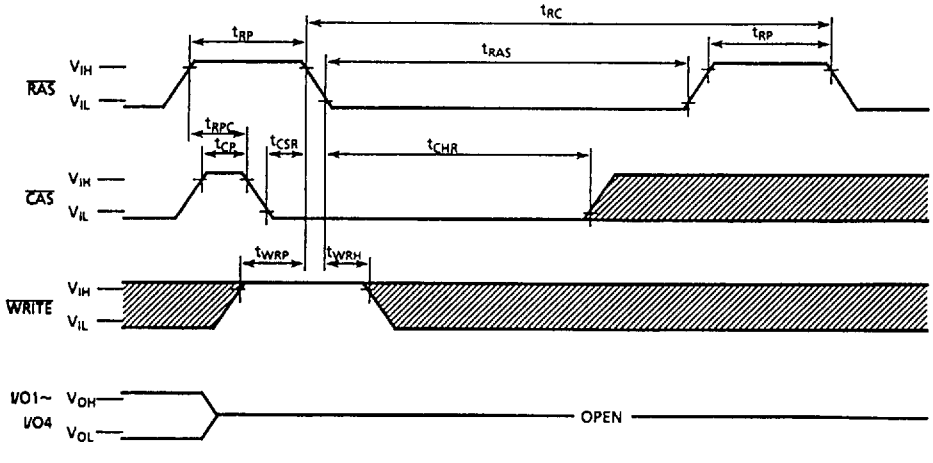
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: D_{IN}, $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"

▨ : "H" or "L"

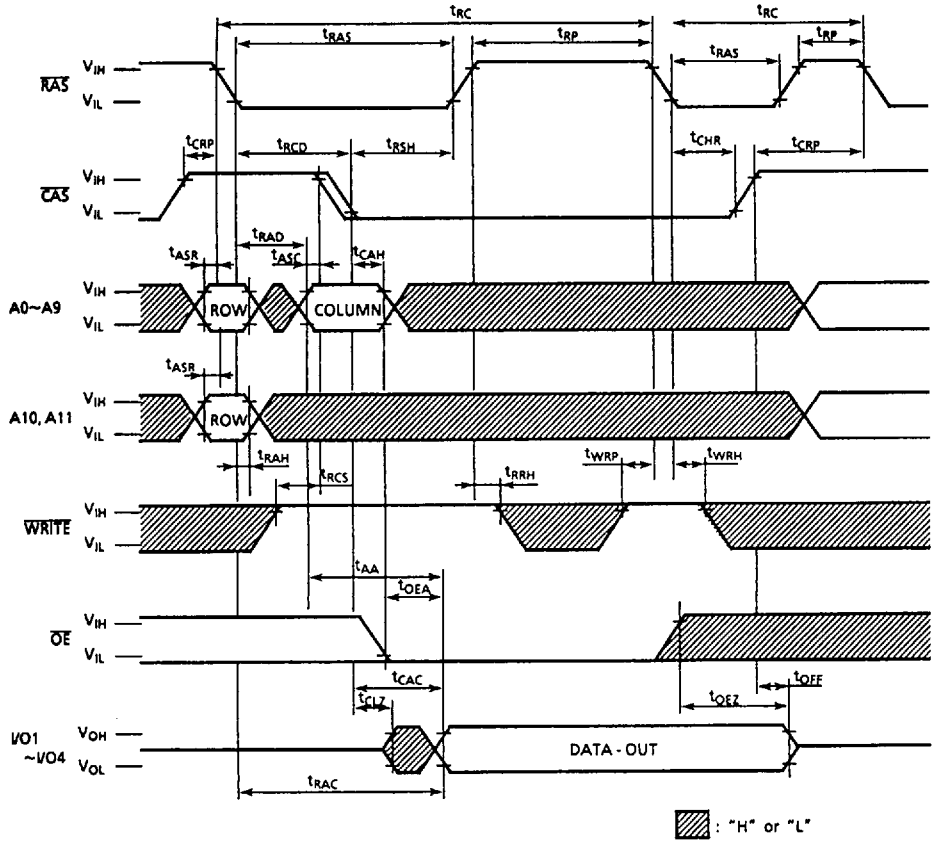
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A11 = "H" or "L"

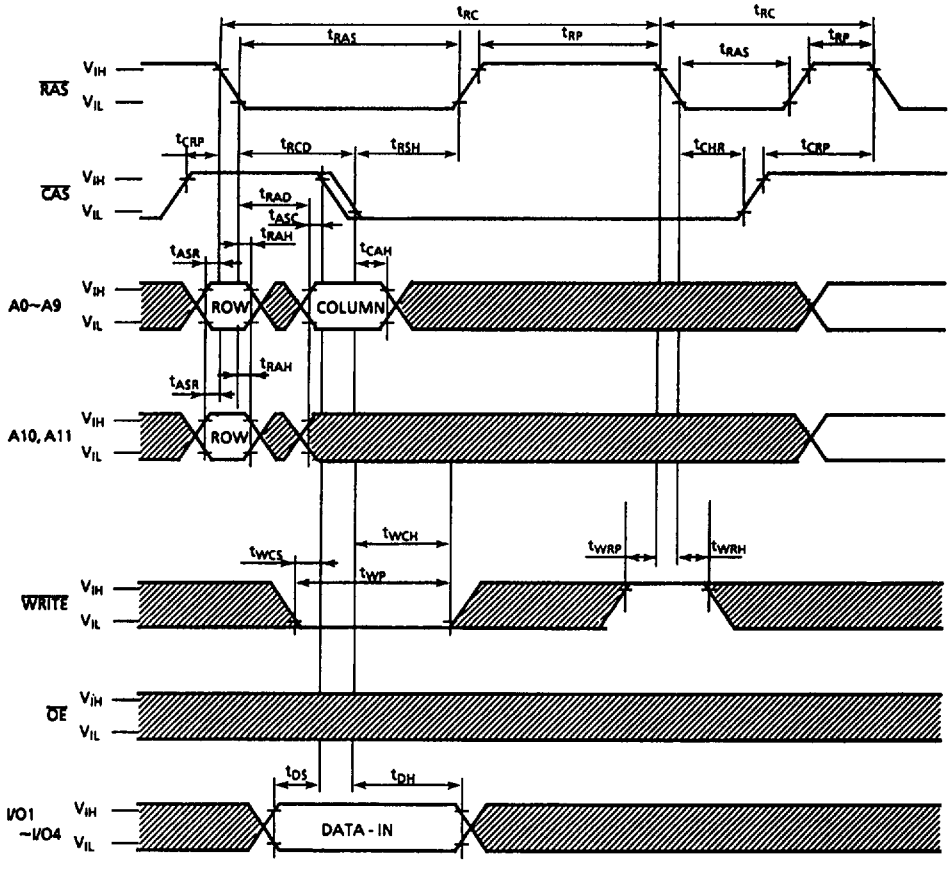
▨ : "H" or "L"

HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

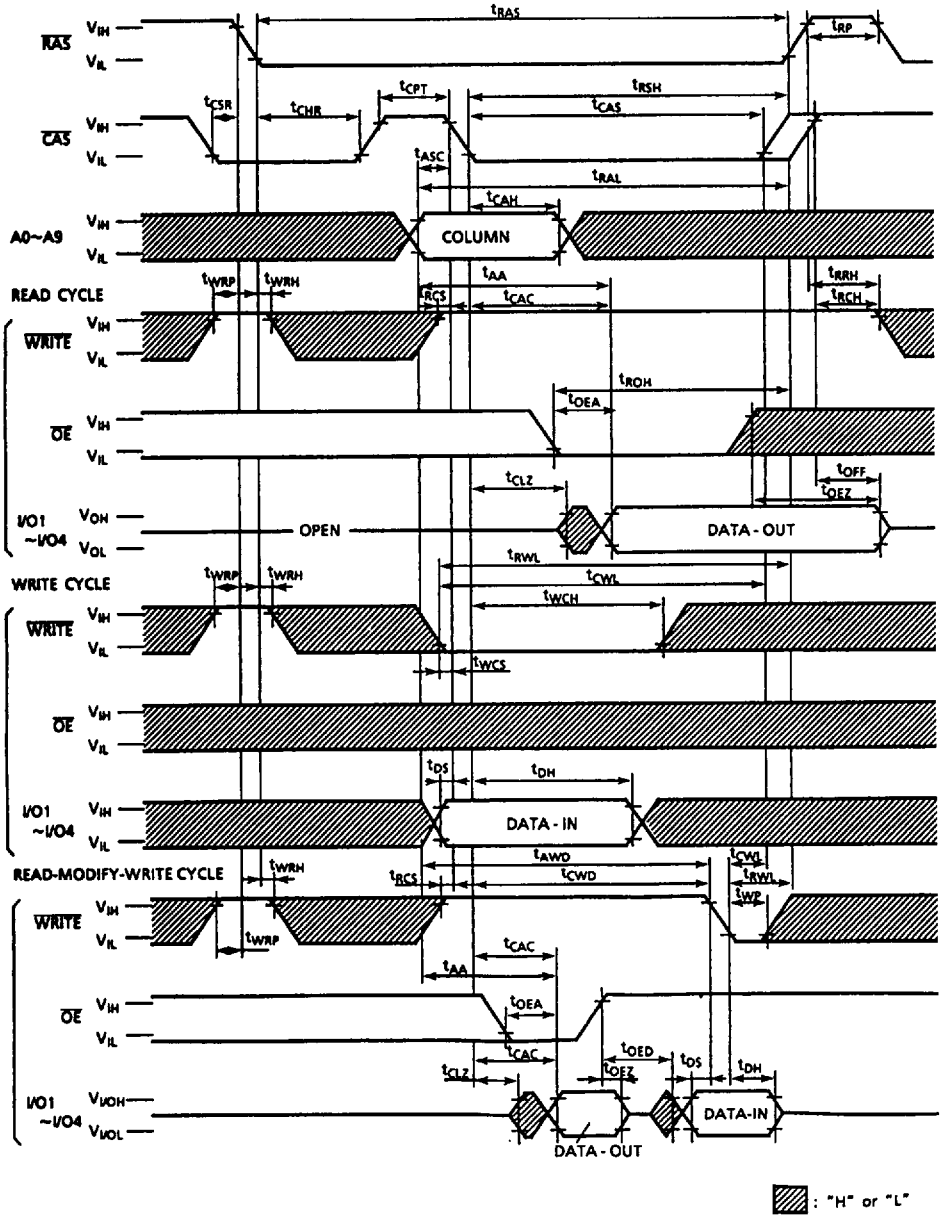
HIDDEN REFRESH CYCLE (WRITE)



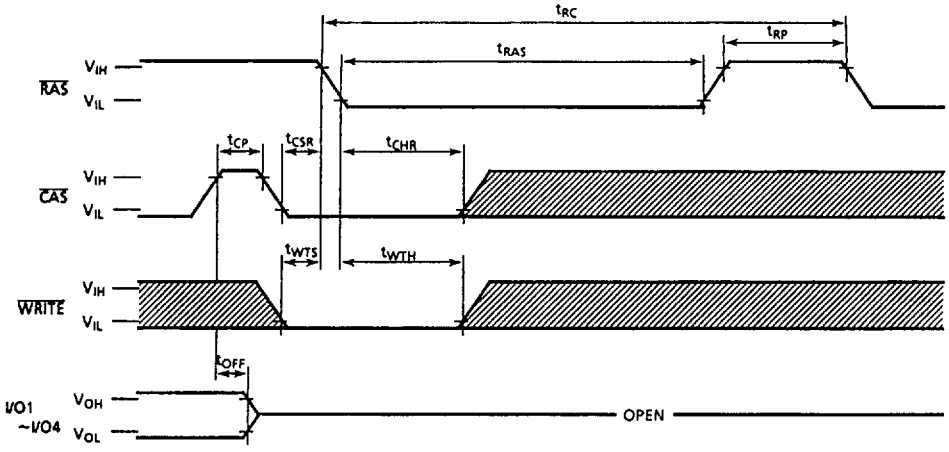
Note: D_{OUT} = OPEN

▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



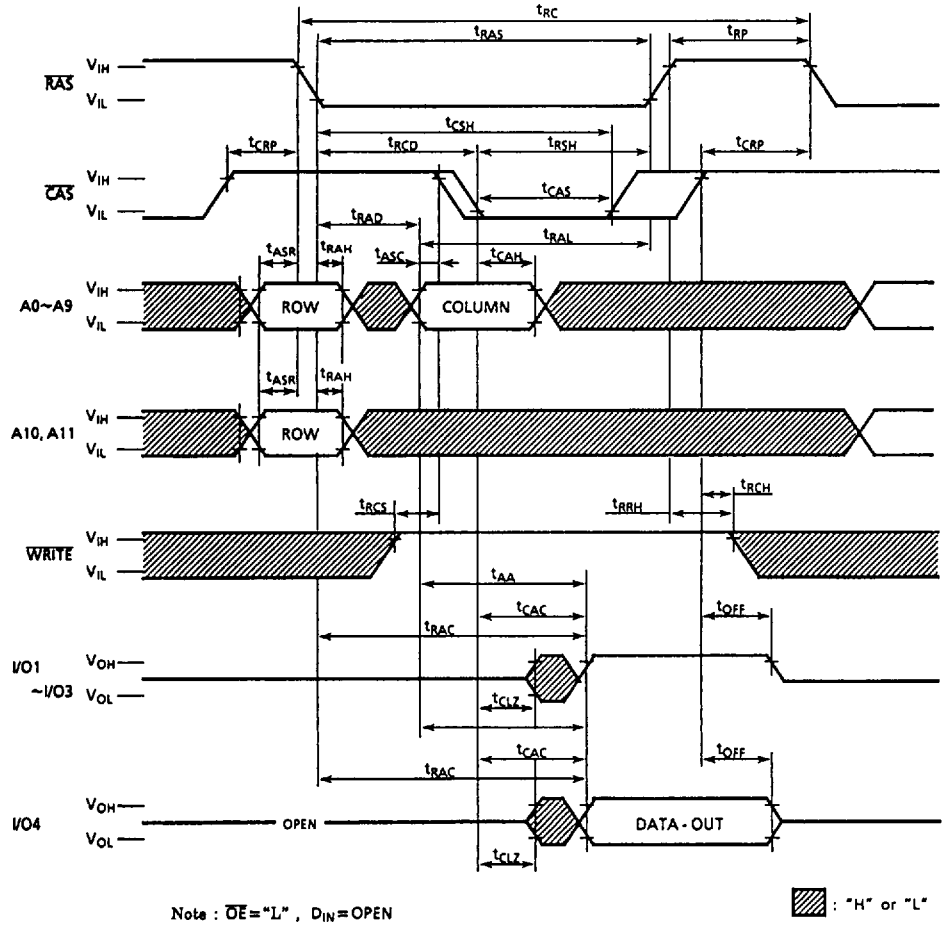
WRITE, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A11 = "H" or "L"

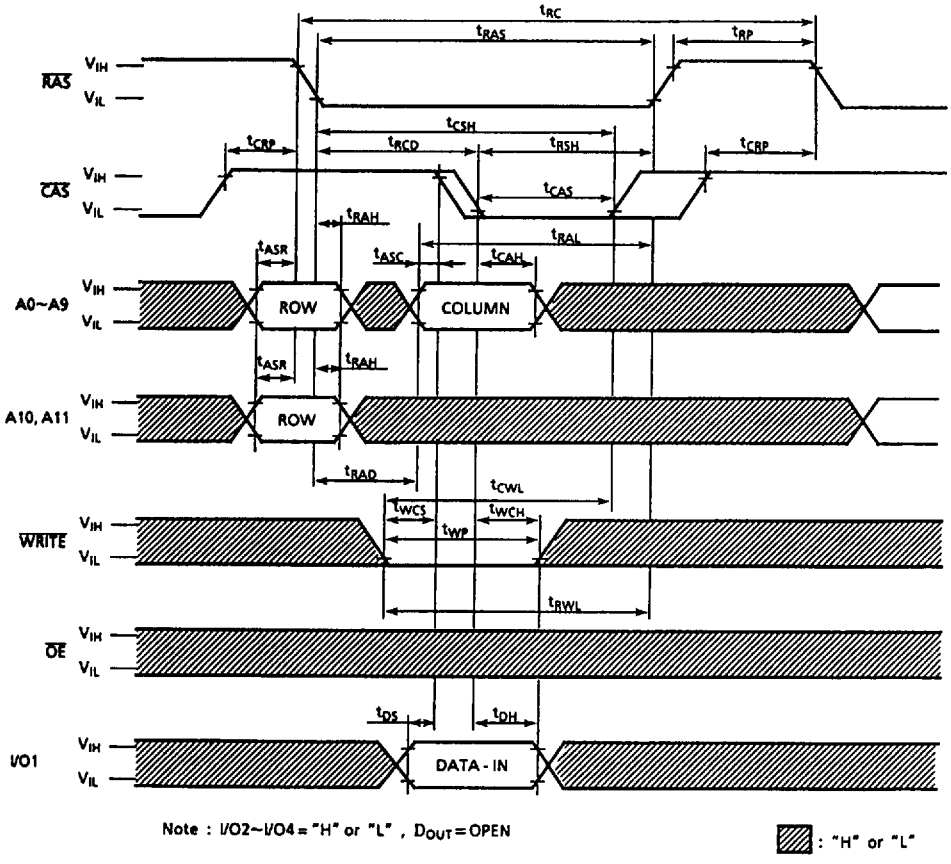
▨ : "H" or "L"

READ CYCLE IN THE TEST MODE



Note : $\overline{OE}$="L", D_{IN}=OPEN

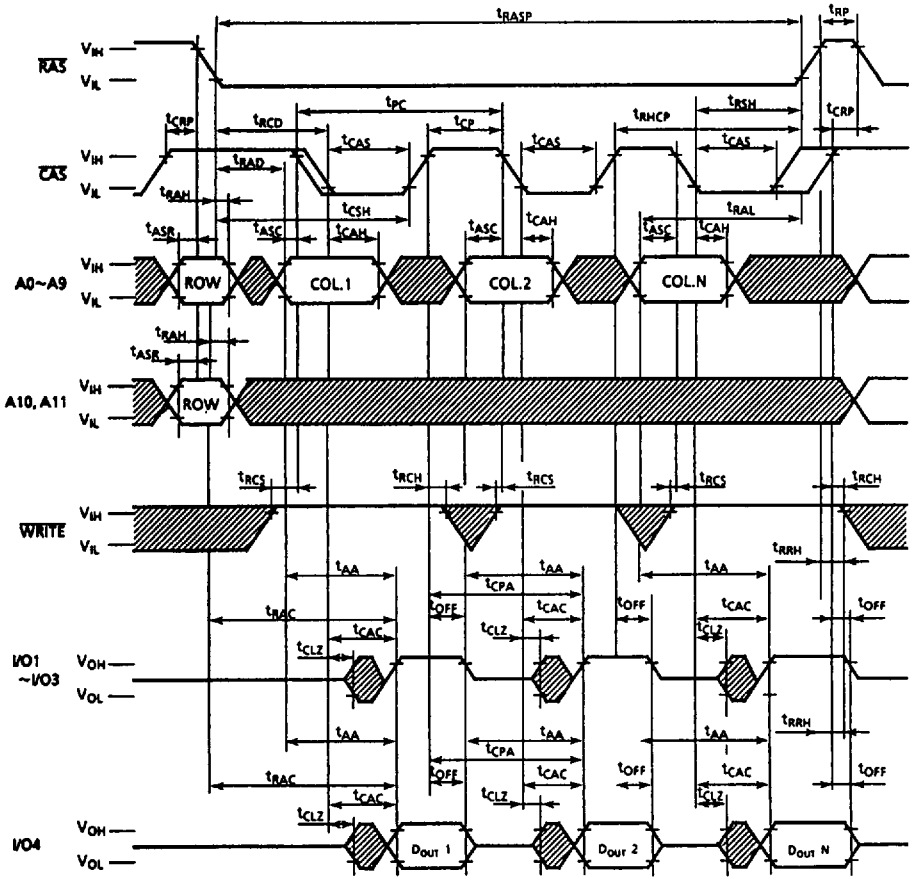
WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



Note : I/O2~I/O4 = "H" or "L" , D_{OUT} = OPEN

▨ : "H" or "L"

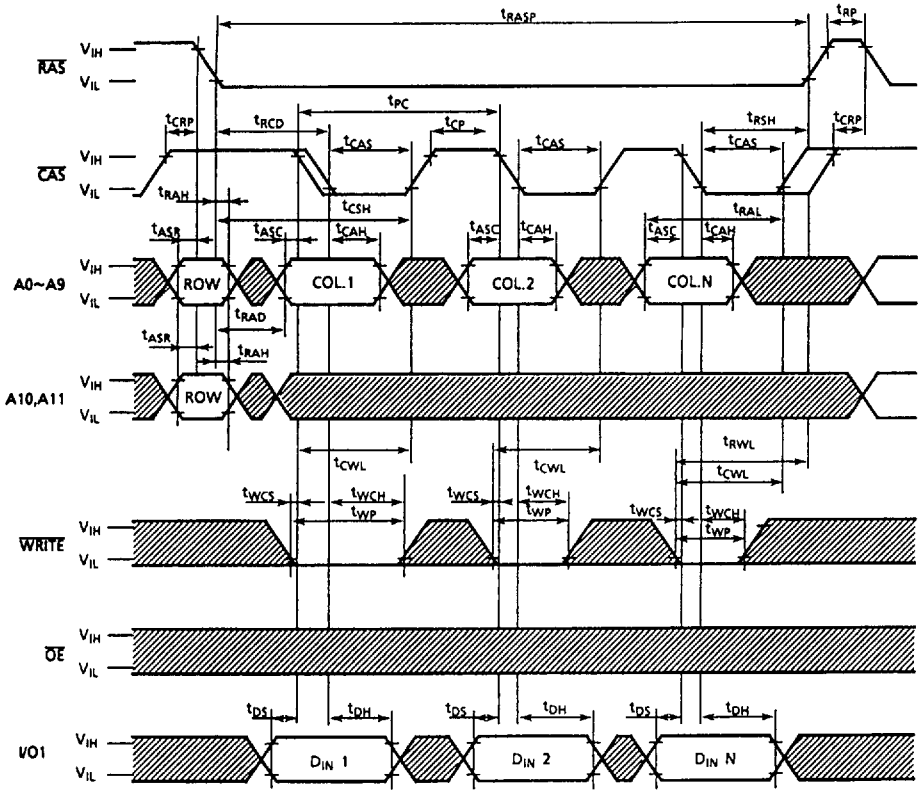
FAST PAGE MODE READ CYCLE IN THE TEST MODE



Note : $\overline{OE}$="L", D_{IN}=OPEN

▨ : "H" or "L"

FAST PAGE MODE WRITE CYCLE IN THE TEST MODE



Note : I/O2~I/O4 = "H" or "L" , D_{OUT} = OPEN

TEST MODE

The TC5116400J/FT is the RAM organized 4,194,304 words by 4 bits, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel by using only I/IO. A1c, A0c are not used. If, upon reading, 16 bits equal (all "1"s or "0"s), the IIO4 pin indicates a"1". If they were not equal, the I/O4 pin would indicate a "0". I/O1, I/O2 and I/O3 always indicate "1" during test mode read cycle. Fig. 1 shows the block diagram of TC5116400J/FT. In "Test Mode", the 4M5DRAM can be tested as if it were a 1M516DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or $\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal refresh address counter. The "Test Mode" function reduces test times (1/4 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

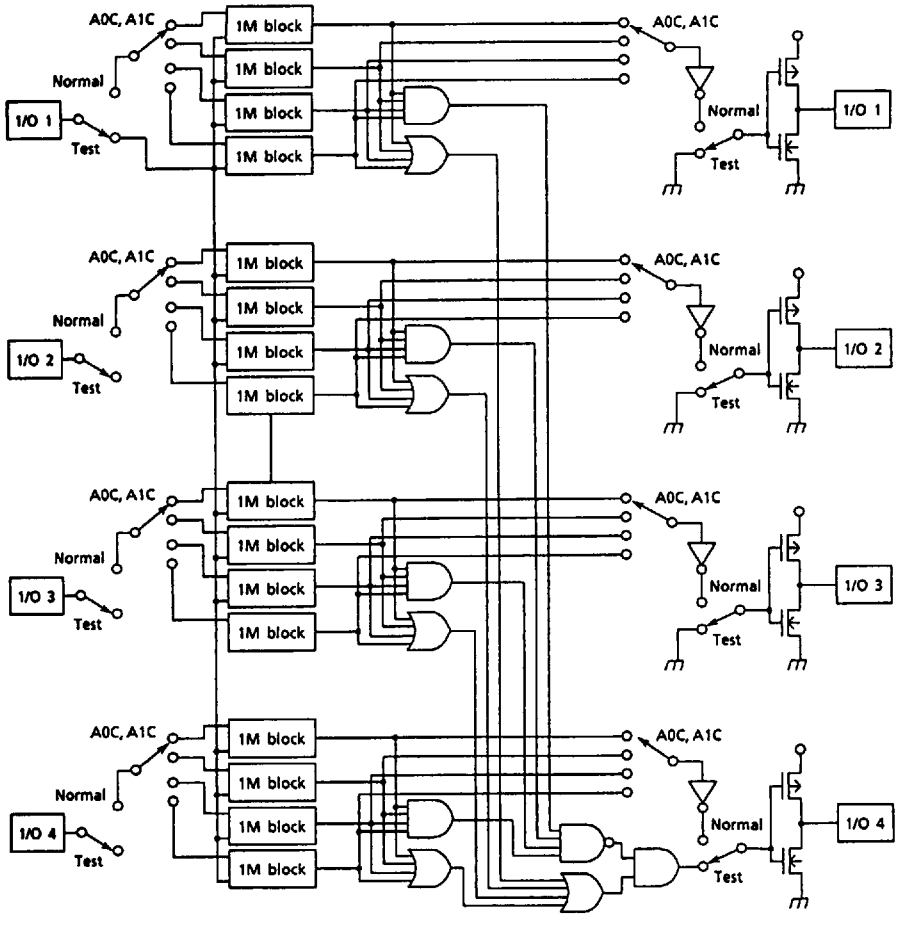


Figure 1